REMARKS

Claims 1-28, and 32-39 are pending in this application. By this Amendment, claims 1-28 and 32-33 are amended, claims 29-31 are canceled, and new claims 34-39 are added. No new matter is added.

The courtesies extended to Applicant's representative by Examiners Sherman and Liang at the interview held on February 1, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicant's record of the interview.

Reconsideration in view of the above amendments and the following remarks is respectfully requested.

I. Objection of the Disclosure

The Office Action Objects to the disclosure due to a minor informality. The specification is amended to obviate the objection. Applicant respectfully requests that the Examiner withdraw the objection.

II. Nonstatutory Double Patenting Rejection

The Office Action provisionally rejects claims 1-33 under the judicially created doctrine of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-23 of Miyazawa (U.S. Patent No. 6,885,029).

A Terminal Disclaimer is filed herewith to obviate the rejection under the judicially created doctrine of double patenting. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection.

III. §112, Second Paragraph, Rejection

The Office Action rejects claims 9 and 26 under 35 U.S.C. §112, second paragraph, as lacking sufficient antecedent basis. Claims 9 and 26 are amended to obviate the rejection. Applicant respectfully requests that the Examiner withdraw the rejection.

IV. Claims Define Patentable Subject Matter

The Office Action rejects claims 17-18 and 29-31 under 35 U.S.C. §102(e) as being anticipated by Akimoto (U.S. Patent Application Publication No. 2003/0067424); rejects claims 1, 4-8, 10, 15-16, 19, 22-25, 27-28, and 32-33 under 35 U.S.C. §103(a) as being unpatentable over Akimoto, in view of Matsumoto (U.S. Patent Application Publication No. 2002/0167504); and rejects claims 2 and 20 under 35 U.S.C. §103(a) as being unpatentable over Akimoto, in view of Matsumoto, and further in view of Okumura (U.S. Patent No. 6,344,850). The §102(e) rejection as it pertains to claims 29-31 is now moot. However, Applicant respectfully traverses the rejections as they pertain to the remainder of the claims.

Specifically, Applicant asserts that neither Akimoto, Matsumoto, nor Okumura disclose or suggest, individually or in combination, an electronic circuit including at least a first power source line, a control circuit that sets a potential of the first power source line to a plurality of potentials or controls an electrical disconnection and an electrical connection between the first power source line and a predetermined voltage, a plurality of unit circuits, each of the plurality of unit circuits including at least a first transistor, a capacitive element having a second electrode, and a third transistor, wherein an electrically conductive state of the first transistor being set during at least a part of a first period in which the data line is electrically connected to the second electrode through the third transistor, as recited in independent claims 1, 11, and 19; or disclose or suggest an electronic circuit including at least a first transistor having a first control terminal, a power source line, and a second transistor having a third terminal that is coupled to the first control terminal and a fourth terminal that is *directly connected to* the power source line, as recited in independent claims 15, 36, and 37.

Akimoto discloses a structure configuration of an OLED display panel having a reset TFT switch connected to a retention capacitor, and the retention capacitor connected to a power supply line. Accordingly, Akimoto does not disclose an electronic circuit including at

least a second transistor having a third terminal that is coupled to the first control terminal and a fourth terminal that is *directly connected to* the power source line, or an electronic circuit including at least a first power source line, a control circuit that sets a potential of the first power source line to a plurality of potentials or controls an electrical disconnection and an electrical connection between the first power source line and a predetermined voltage, a plurality of unit circuits, each of the plurality of unit circuits including at least a first transistor, a capacitive element having a second electrode, and a third transistor, wherein an electrically conductive state of the first transistor being set during at least a part of a first period in which the data line is electrically connected to the second electrode through the third transistor.

Matsumoto discloses a driving circuit including an RGB selection circuit for generating signals for selectively driving data line switches. Accordingly, Matsumoto also fails to disclose an electronic circuit including at least a second transistor having a third terminal that is coupled to the first control terminal and a fourth terminal that is *directly connected to* the power source line, or an electronic circuit including at least a first power source line, a control circuit that sets a potential of the first power source line to a plurality of potentials or controls an electrical disconnection and an electrical connection between the first power source line and a predetermined voltage, a plurality of unit circuits, each of the plurality of unit circuits including at least a first transistor, a capacitive element having a second electrode, and a third transistor, wherein an electrically conductive state of the first transistor being set during at least a part of a first period in which the data line is electrically connected to the second electrode through the third transistor.

Okumura discloses an a holding circuit for holding image data reconstructed on the basis of differential data received from a data transmitting section to delay the image data by a predetermined period, and an addition circuit for reconstructing a present image data by

adding a previous image data delayed by the holding circuit to the differential data received from the data transmitting section. Accordingly, Okumura also fails to disclose at least the aforementioned features of claims 1, 11, 15, 19, 36, and 37, and therefore, does not make up for the deficiencies of Akimoto or Matsumoto

Accordingly, Applicant respectfully asserts that neither Akimoto, Matsumoto, nor Okumura disclose or suggest, individually or in combination, an electronic circuit including at least a first power source line, a control circuit that sets a potential of the first power source line to a plurality of potentials or controls an electrical disconnection and an electrical connection between the first power source line and a predetermined voltage, a plurality of unit circuits, each of the plurality of unit circuits including at least a first transistor, a capacitive element having a second electrode, and a third transistor, wherein an electrically conductive state of the first transistor being set during at least a part of a first period in which the data line is electrically connected to the second electrode through the third transistor, or disclose or suggest an electronic circuit including at least a first transistor having a first control terminal, a power source line, and a second transistor having a third terminal that is coupled to the first control terminal and a fourth terminal that is *directly connected to* the power source line.

In accordance with the above remarks, Applicant submits that independent claims 1, 11, 15, 19, 36, and 37 define patentable subject matter. Claims 2-10, 12-14, 16-18, 20-28, 32-35, and 38-39 depend from claims 1, 11, 15, and 19, respectively, and therefore, also define patentable subject matter. Thus, Applicants respectfully request that the Examiner withdraw the §102(e) and §103(a) rejections.

V. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-28 and 32-39 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Bogdan A. Zinchenko
Registration No. 57,473

JAO:BAZ/hs

Attachment:
Amendment Transmittal
Terminal Disclaimer

Date: February 16, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461